BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

As rescanning documents *will not* correct images, please do not report the images to the Image Problem Mailbox.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/821,554	03/29/2001	Weng Chang	67,200-367	5869

7590 04/22/2003

TUNG & ASSOCIATES
838 W. Long Lake Road, Suite 120
Bloomfield Hills, MI 48302

EXAMINER
UMEZ ERONINI, LYNETTE T

ART UNIT	PAPER NUMBER
1765	12

DATE MAILED: 04/22/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/821,554	CHANG ET AL.
	Examiner	Art Unit
	Lynette T. Umez-Eronini	1765

-- The MAILING DATE of this communication appears on th cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-15 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-15 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Pri rity under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 1 and 3 are rejected under 35 U.S.C. 102(e) as being anticipated by Somekh (US 6,292,334 B1).

As pertaining to claim 1, Somekh teaches a method of forming an aperture through a dielectric layer. The method comprises:

"A dual damascene structure . . . in FIG. ***4h*** . . . and the method of making the structure . . . in FIGS. ***4a-4h***, which are cross sectional views of a substrate . . ." (column 3, lines 36-38 and FIGS. **4a-4f**), which reads on,

providing a substrate;

As shown in FIG. ***4b***, a low k etch stop **14** (same as applicant's first dielectric layer), such as . . . α-FC . . . Low k etch stop **14** (same as applicant's first dielectric

layer) is then pattern etched to define the contact/via openings **16** . . ." (column 3, lines 42-47) and " . . . α-FC (dielectric constant ~2.8) . . ." (column 4, lines 15-16), which reads on,

forming upon the substrate a patterned first dielectric layer formed of a first dielectric material having a first dielectric constant of less than about 4.0, the patterned first dielectric layer defining a via.

Somekh teaches, "After low k etch stop **14** (same as applicant's first dielectric layer) has been etched to pattern the contacts/vias and the photoresist has been removed, a second dielectric layer **18** (same as applicant's blanket second dielectric layer) is deposited over the etch stop **14** (same as applicant's first dielectric layer) . . . as shown in FIG. **4***d*. Second dielectric layer **18** (same as applicant's blanket second dielectric layer) is then patterned to define interconnect lines **20**, . . . with a photoresist layer **22** (same as applicant's patterned mask layer, which defines the location of a trench to be formed through the blanket second dielectric layer) as shown in FIG. **4***e*" (column 3, lines 52-59; FIG. **4c** and **4d**; column 4, lines 15-16, 62-63; and FIG. **4e**), which reads on,

forming upon the patterned first dielectric layer and filling the via a blanket second dielectric material formed of a second dielectric material having a second dielectric constant of less than about 4.0.

Somekh further teaches, "The interconnects and contacts/vias are then etched using reactive ion etching or other anisotropic etching techniques to define the

metallization structure (i.e., the interconnect and contact/via) as shown in FIG. **4f'** (column 3, lines 59-63), which reads on,

forming over the blanket second dielectric layer a patterned mask layer which defines the location of a trench to be formed through the blanket second dielectric layer, where an areal dimension of the trench is greater than at least in part overlapping an areal dimension of the via (column 3, lines 54-63 and column 4, lines 63-66);

etching, while employing the patterned mask layer, in conjunction with an anisotropic etch method, the blanket second dielectric layer to form an aperture comprising: the trench; and

at least a portion of the via, where the patterned first dielectric layer provides an intrinsic etch stop within the anisotropic etch method.

Somekh also teaches:

the α-FC etch stop layer and the second α-FC layer (column 4, lines 31-32 and column 4, lines 62-66), and the α-FC has a dielectric constant of ~2.8 (column 4, lines 15-16), and further teaches alternative carbon based films such as parylene (column 3, lines 43-46 and column 5, lines 33-41), which read on the patterned first dielectric layer and the blanket second dielectric layer are formed from a separate dielectric material selected from the group consisting of amorphous carbon dielectric materials, as in **claim 3.**

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Somekh ('334B1) as applied to claim 1 above, and further in view of Yu et al. (US 6,004,883).

Somekh differs in failing to specify the microelectronic fabrication selected group wherein a substrate is employed, in **claim 2**.

Yu teaches, "a substrate employed within a microelectronics fabrication including but not limited to a semiconductor integrated circuit microelectronics fabrication, . . ." (column 7, lines 38).

It is the examiner's position that it would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Somekh by using the microelectronic fabrication method as taught by Yu for the purpose forming within a microelectronics fabrications low dielectric constant dielectric layers interposed between the patterns of patterned conductor layers which in turn contact patterned conductor stud layers, with attenuated process complexity (column 4, lines 50-54 and column 6, lines 6-11).

Claim R j ctions - 35 USC § 102

5. Claims 4 and 7 are rejected under 35 U.S.C. 102(e) as being anticipated by Somekh (US 6,292,334 B1).

As pertaining to claim 4, Somekh teaches a method of forming an aperture through a dielectric layer. The method comprises:

"A dual damascene structure . . . in FIG. ***4h*** . . . and the method of making the structure . . . in FIGS. ***4a-4h***, which are cross sectional views of a substrate . . ." (column 3, lines 36-38 and FIGS. **4a-4f**), which reads on,

providing a substrate;

As shown in FIG. ***4b***, a low k etch stop **14** (same as applicant's first dielectric layer), such as . . . α-FC . . . Low k etch stop **14** (same as applicant's first dielectric layer) is then pattern etched to define the contact/via openings **16** . . ." (column 3, lines 42-47) and " . . . α-FC (dielectric constant ~2.8) . . ." (column 4, lines 15-16), which reads on,

forming upon the substrate a patterned first dielectric layer formed of a first dielectric material having a first dielectric constant of less than about 4.0, the patterned first dielectric layer defining a via.

Somekh teaches, "After low k etch stop **14** (same as applicant's first dielectric layer) has been etched to pattern the contacts/vias and the photoresist has been removed, a second dielectric layer **18** (same as applicant's blanket second dielectric layer) is deposited over the etch stop **14** (same as applicant's first dielectric layer) . . . as shown in FIG. ***4d***. Second dielectric layer **18** (same as applicant's blanket second

dielectric layer) is then patterned to define interconnect lines **20**, . . . with a photoresist layer **22** (same as applicant's patterned mask layer, which defines the location of a trench to be formed through the blanket second dielectric layer) as shown in FIG. **4***e*" (column 3, lines 52-59; FIG. **4c** and **4d**; column 4, lines 15-16, 62-63; and FIG. **4e**), which reads on,

forming upon the patterned first dielectric layer and filling the via a blanket second dielectric material formed of a second dielectric material having a second dielectric constant of less than about 4.0.

One can see that FIG. **4***f* lack**s** a layer between **14** (same as applicant's patterned first dielectric layer) and layer **18** (same as applicant's blanket second dielectric layer), which reads on,

wherein an extrinsic hard mask is not formed interposed between the patterned first dielectric layer and the blanket second dielectric layer.

Somekh further teaches, "The interconnects and contacts/vias are then etched using reactive ion etching or other anisotropic etching techniques to define the metallization structure (i.e., the interconnect and contact/via) as shown in FIG. **4***f*" (column 3, lines 59-63), which reads on,

forming over the blanket second dielectric layer a patterned mask layer which defines the location of a trench to be formed through the blanket second dielectric layer, where an areal dimension of the trench is greater than at least in part overlapping an areal dimension of the via;

etching, while employing the patterned mask layer, in conjunction with an anisotropic etch method, the blanket second dielectric layer to form an aperture comprising: the trench; and

at least a portion of the via, where the patterned first dielectric layer provides an intrinsic etch stop within the anisotropic etch method.

Somekh also teaches, "A second photoresist layer is then deposited on the second FSG layer and exposed . . ." (column 4, lines 63-66), which reads on, the patterned mask layer is selected from the group consisting of patterned photoresist mask layers, **in claim 7**.

Claim Rejections - 35 USC § 103

6. Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Somekh ('334B1) as applied to claim 4 above, and further in view of Yu et al. (US 6,004,883).

Somekh differs in failing to specify the dielectric layer is formed to a thickness from 4000 to 10,000 angstroms, in **claim 5** and the dielectric layer is formed to a thickness of from about 4000 to about 7000 angstroms, in **claim 6**.

Yu teaches a dielectric layer having a thickness of from 5000 to about 9000 angstroms (column 7, lines 55-58), which falls within the range of 4000 and 10,000 angstroms.

Hence it is the examiner's position that it would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Somekh by using a dielectric layer having a thickness as taught by Yu for the purpose of forming within a microelectronics fabrications low dielectric constant dielectric layers interposed between the patterns of patterned conductor layers which in turn contact patterned conductor stud layers, with attenuated process complexity (column 4, lines 50-54 and column 6, lines 6-11).

Claim Rejections - 35 USC § 102

7. Claims 8 and 10 are rejected under 35 U.S.C. 102(e) as being anticipated by Somekh (US 6,292,334 B1).

As pertaining to claim 8, Somekh teaches a method of forming a patterned conductor layer within an aperture through a dielectric layer. The method comprises:

"A dual damascene structure . . . in FIG. ***4h*** . . . and the method of making the structure . . . in FIGS. ***4a-4h***, which are cross sectional views of a substrate . . ." (column 3, lines 36-38 and FIGS. **4a-4f**), which reads on,

providing a substrate;

As shown in FIG. ***4b***, a low k etch stop **14** (same as applicant's first dielectric layer), such as . . . α-FC . . . Low k etch stop **14** (same as applicant's first dielectric layer) is then pattern etched to define the contact/via openings **16** . . ." (column 3, lines 42-47) and " . . . α-FC (dielectric constant ~2.8) . . ." (column 4, lines 15-16), which reads on,

forming upon the substrate a patterned first dielectric layer formed of a first dielectric material having a first dielectric constant of less than about 4.0, the patterned first dielectric layer defining a via.

Somekh teaches, "After low k etch stop **14** (same as applicant's first dielectric layer) has been etched to pattern the contacts/vias and the photoresist has been removed, a second dielectric layer **18** (same as applicant's blanket second dielectric layer) is deposited over the etch stop **14** (same as applicant's first dielectric layer) . . . as shown in FIG. **4***d*. Second dielectric layer **18** (same as applicant's blanket second dielectric layer) is then patterned to define interconnect lines **20**, . . . with a photoresist layer **22** (same as applicant's patterned mask layer, which defines the location of a trench to be formed through the blanket second dielectric layer) as shown in FIG. **4***e*" (column 3, lines 52-59; FIG. **4c** and **4d**; column 4, lines 15-16, 62-63; and FIG. **4**), which reads on,

forming upon the patterned first dielectric layer and filling the via a blanket second dielectric material formed of a second dielectric material having a second dielectric constant of less than about 4.0.

Somekh further teaches, "The interconnects and contacts/vias are then etched using reactive ion etching or other anisotropic etching techniques to define the metallization structure (i.e., the interconnect and contact/via) as shown in FIG. **4***f*" (column 3, lines 59-63), which reads on,

forming over the blanket second dielectric layer a patterned mask layer which defines the location of a trench to be formed through the blanket second dielectric layer,

where an areal dimension of the trench is greater than at least in part overlapping an areal dimension of the via;

etching, while employing the patterned mask layer, in conjunction with an anisotropic etch method, the blanket second dielectric layer to form an aperture comprising: the trench; and

at least a portion of the via, where the patterned first dielectric layer provides an intrinsic etch stop.

Somekh further teaches, "the patterned dual damascene structure (same as applicant's contiguous patterned conductor interconnect and patterned conductor stud layer) . . . is filled with copper" (column 5, lines 15-18 and FIG. **4*h***), which reads on,

forming within the aperture a contiguous patterned conductor interconnect and patterned conductor stud layer.

Somekh also teaches:

the α-FC etch stop layer and the second α-FC layer (column 4, lines 31-32 and column 4, lines 62-66), and the α-FC has a dielectric constant of ~2.8 (column 4, lines 15-16), and further teaches alternative carbon based films such as parylene (column 3, lines 43-46 and column 5, lines 33-41), which read on the patterned first dielectric layer and the blanket second dielectric layer are formed from a separate dielectric material selected from the group consisting of amorphous carbon dielectric materials, as in **claim 10**.

Claim R j ctions - 35 USC § 103

8. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Somekh ('334B1) as applied to claims 1 and 8 respectively above, and further in view of Yu et al. (US 6,004,883).

Somekh differs in failing to specify the microelectronic fabrication is selected from the group wherein a substrate is employed, in **claim 9**.

Yu teaches, "a substrate employed within a microelectronics fabrication including but not limited to a semiconductor integrated circuit microelectronics fabrication, . . ." (column 7, lines 38).

It is the examiner's position that it would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Somekh by using the microelectronic fabrication method as taught by Yu for the purpose forming within a microelectronics fabrications low dielectric constant dielectric layers interposed between the patterns of patterned conductor layers which in turn contact patterned conductor stud layers, with attenuated process complexity (column 4, lines 50-54 and column 6, lines 6-11).

Claim Rejections - 35 USC § 102

9. Claims 11, 14, and 15 are rejected under 35 U.S.C. 102(e) as being anticipated by Somekh (US 6,292,334 B1).

As pertaining to claim 8, Somekh teaches a method of forming a patterned conductor layer within an aperture through a dielectric layer. The method comprises:

"A dual damascene structure . . . in FIG. **4*h*** . . . and the method of making the structure . . . in FIGS. **4*a*-4*h***, which are cross sectional views of a substrate . . ." (column 3, lines 36-38 and FIGS. **4a-4f**), which reads on,

providing a substrate;

As shown in FIG. **4*b***, a low k etch stop **14** (same as applicant's first dielectric layer), such as . . . α-FC . . . Low k etch stop **14** (same as applicant's first dielectric layer) is then pattern etched to define the contact/via openings **16** . . ." (column 3, lines 42-47) and " . . . α-FC (dielectric constant ~2.8) . . ." (column 4, lines 15-16), which reads on,

forming upon the substrate a patterned first dielectric layer formed of a first dielectric material having a first dielectric constant of less than about 4.0, the patterned first dielectric layer defining a via.

Somekh teaches, "After low k etch stop **14** (same as applicant's first dielectric layer) has been etched to pattern the contacts/vias and the photoresist has been removed, a second dielectric layer **18** (same as applicant's blanket second dielectric layer) is deposited over the etch stop **14** (same as applicant's first dielectric layer) . . . as shown in FIG. **4*d***. Second dielectric layer **18** (same as applicant's blanket second dielectric layer) is then patterned to define interconnect lines **20**, . . . with a photoresist layer **22** (same as applicant's patterned mask layer, which defines the location of a trench to be formed through the blanket second dielectric layer) as shown in FIG. **4*e***" (column 3, lines 52-59; FIG. **4c** and **4d**; column 4, lines 15-16, 62-63; and FIG. **4e**), which reads on,

forming upon the patterned first dielectric layer and filling the via a blanket second dielectric material formed of a second dielectric material having a second dielectric constant of less than about 4.0;

One can see that FIG. ***4f*** lacks a layer between **14** (same as applicant's patterned first dielectric layer) and layer **18** (same as applicant's blanket second dielectric layer), which reads on,

wherein an extrinsic hard mask is not formed interposed between the patterned first dielectric layer and the blanket second dielectric layer.

Somekh further teaches, "The interconnects and contacts/vias are then etched using reactive ion etching or other anisotropic etching techniques to define the metallization structure (i.e., the interconnect and contact/via) as shown in FIG. ***4f***" (column 3, lines 59-63), which reads on,

forming over the blanket second dielectric layer a patterned mask layer which defines the location of a trench to be formed through the blanket second dielectric layer, where an areal dimension of the trench is greater than at least in part overlapping an areal dimension of the via;

etching, while employing the patterned mask layer, in conjunction with an anisotropic etch method, the blanket second dielectric layer to form an aperture comprising: the trench; and

at least a portion of the via, where the patterned first dielectric layer provides an intrinsic etch stop within the anisotropic etch method.

Somekh teaches, "the patterned dual damascene structure (same as applicant's contiguous patterned conductor interconnect and patterned conductor stud layer) . . . is filled with copper" (column 5, lines 15-18 and FIG. ***4h***), which reads on,

forming within the aperture a contiguous patterned conductor interconnect and patterned conductor stud layer is formed within the aperture.

Somekh also teaches:

"A second photoresist layer is then deposited on the second FSG layer and exposed . . ." (column 4, lines 63-66), which reads on,

a photoresist layer is formed over the α-FC etch stop layer and the second α-FC layer (column 4, lines 46-48 and column 4, lines 63-66), which reads on the patterned mask layer is selected from the group consisting of patterned photoresist mask layers, **in claim 14** and

"The metal layer is then planarized by chemical mechanical polishing . . ." (column 5, lines 24-27), which reads on the contiguous patterned conductor interconnect and patterned conductor stud layer is formed within the aperture while employing a chemical mechanical polish (CMP) planarizing method, as **in claim 15**.

Claim Rejections - 35 USC § 103

10. Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Somekh ('334B1) as applied to claim 11 above, and further in view of Yu et al. (US 6,004,883).

Somekh differs in failing to specify the dielectric layer is formed to a thickness from 4000 to 10,000 angstroms, in **claim 12** and the dielectric layer is formed to a thickness of from about 4000 to about 7000 angstroms, in **claim 13**.

Yu teaches a dielectric layer having a thickness of from 5000 to about 9000 angstroms (column 7, lines 55-58), which falls within the range of 4000 and 10,000 angstroms.

Hence it is the examiner's position that it would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Somekh by using a dielectric layer having a thickness as taught by Yu for the purpose of forming within a microelectronics fabrications low dielectric constant dielectric layers interposed between the patterns of patterned conductor layers which in turn contact patterned conductor stud layers, with attenuated process complexity (column 4, lines 50-54 and column 6, lines 6-11).

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lynette T. Umez-Eronini whose telephone number is 703-306-9074. The examiner is normally unavailable on the First Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Benjamin Utech can be reached on 703-308-3836. The fax phone numbers for the organization where this application or proceeding is assigned are 703-972-9310 for regular communications and 703-972-9311 for After Final communications.

ltue
April 18, 2003

BENJAMIN L. UTECH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 1700